

BitTracer™ Logic Display for PCI Express®

View Physical
Layer Logic
Signals on a
Protocol
Analyzer!!

The BitTracer Logic Display is a software option that runs on the Teledyne LeCroy Summit™ PCI Express Protocol Analyzers. BitTracer offers developers a physical layer view of PCI Express traffic, similar to what might be displayed on a logic analyzer, but provides this capability on a protocol analyzer. This means that developers can view bit stream traffic before it is decoded to high-level packets, to better understand where signal integrity issues may be causing data corruption.

Typical product development in the lab often requires both a logic analyzer and protocol analyzer to work in tandem to solve issues. Unfortunately, logic analyzers may need to be repeatedly taken off and laboriously hooked back up to make measurements. The BitTracer Logic Display helps eliminate this problem by having one piece of equipment that can display the logic analyzer state listing (as the logic analyzer does), but still show the high-level packet information that a protocol analyzer does. Symbol, 10b, scrambled, or unscrambled data can be viewed and correlated to high-level packet traces. This gives developers the best of both worlds, maintaining a focus on solving the problem instead of wasting time with the long process of changing the equipment setup.

The BitTracer option is available for all Summit PCI Express Analyzers. The software interface displays a “raw mode” view of all bits in the bit stream for each individual lane. These bits are delineated to the user as they

in the multi-stripped bit stream. Two additional views show the high-level packet decoding created from the delineated bits, either as the familiar CATC Trace™ packet display or showing the packet layout as defined in the PCI Express Specification. These windows correlate together as a user moves through the bit stream showing clearly the nature of any corrupted packets. The BitTracer software also has tools that allow searching, data manipulation and traffic summaries of traces recorded on any Teledyne LeCroy Summit PCI Express Analyzer.



The screenshot displays the BitTracer software interface with several key features highlighted by callouts:

- Change Data Display:** A dropdown menu at the top right allows switching between data representations: 0x, 10b, RD, and Bin.
- Sync Header:** A callout points to the synchronization header in the bit stream data.
- Upstream Lanes:** A callout points to the lanes used for upstream traffic.
- Downstream Lanes:** A callout points to the lanes used for downstream traffic.
- Change Polarity Per Lane:** A callout points to the 'Invert Polarity' checkbox in the Link configuration dialog.
- Change Skew Per Lane:** A callout points to the 'Skew' field in the Link configuration dialog.
- Change Scrambling:** A callout points to the 'Scrambling' options (Disabled, Base Spec 1.0, Base Spec 1.0a) in the Link configuration dialog.
- All Byte Info:** A callout points to a tooltip showing details for a specific byte, including 'Descrambled Byte', 'Scrambled Byte', and 'LFSR'.
- Low Level Decode of Packet:** A callout points to the raw bit stream data.
- High Level Decode of Packet:** A callout points to the decoded packet information at the bottom of the interface.

The interface also includes a menu bar (File, Setup, Record, Generate, Edit, Markers, Search, View, Tools, Window, Help), a toolbar, and a status bar at the bottom showing decoding options (logical, spec).

Key Features and Benefits

- Find signal integrity issues fast using the correlated bit stream packet view
- Reduce setup time by using one piece of equipment instead of two
- Discover difficult-to-find intermittent lane errors

Host Machine Requirements

- Microsoft Windows® 8, Windows Server 2012, Windows 7, Windows Server 2008R2, Windows XP; 2 GB of RAM (16 GB recommended); Storage with at least 1 GB of free space for the installation of the software and additional space for recorded data; display with resolution of at least 1024x768 with at least 16-bit color depth; and USB 2.0 or 10/100/1000 Ethernet. For optimal performance, please refer to our recommended configuration in the product documentation.
- Summit Series Protocol Analyzer

Key Feature Highlights

- Gen1/Gen2/Gen3 (if supported by analyzer)
- x1-x16 lane support (if supported by analyzer)
- Errors Traffic Summary
- Symbol Traffic Summary

Key Feature Highlights (cont...)

- Timing Measurement Display
- Display Modes
 - 10-bit Codes
 - Symbol Decoding
 - Scrambled Bytes
 - Unscrambled Bytes
- Editing Functionality (after capture)
 - Link Width
 - Lane Swizzling
 - Lane Skew
 - Polarity Inversion
 - Scrambling Mode
- Export to Trace
- Color Coding in Raw View
 - All Special Symbols
 - Error Highlighting
- Tool Tips Show Breakdown for Each Symbol
- User Markers
- Triggering

System Compatibility	
Summit T3-16	✓
Summit T3-8	✓
Summit T34	✓
Summit T28	✓
Summit T24	✓

Ordering Information

Product Description

- BitTracer Software Option for Summit T3-16 Analyzer
- BitTracer Software Option for Summit T3-8 Analyzer
- BitTracer Software Option for Summit T34 Analyzer
- BitTracer Software Option for Summit T28 Analyzer
- BitTracer Software Option for Summit T24 Analyzer
- Summit T3-16 (licensed as a Gen3 x16 analyzer, no probes or cables)
- Summit T3-8 (licensed as a Gen3 x8 analyzer, no probes or cables)
- Summit T34 (licensed as a Gen3 x4 analyzer, no probes or cables)
- Summit T28 (licensed as a Gen2 x8 analyzer, no probes or cables)
- Summit T24 (licensed as a Gen2 x4 analyzer, no probes or cables)

Product Code

- PE047SUA-X
- PE077SUA-X
- PE090SUA-A
- PE078SUA-X
- PE082SUA-X
- PE050AAA-X
- PE060AAA-X
- PE080AAA-X
- PE070AAA-X
- PE076AAA-X



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